

OVERVIEW

The 5056 series are 70 to 135MHz oscillation frequency, crystal oscillator module ICs optimized for 3rd overtone crystal elements with C_0 2 to 4pF. They have built-in C_0 cancelation circuit which provides high oscillation performance at high frequency. They also have CMOS output buffer which can drive 30pF output load.

FEATURES

- Operating supply voltage range: 2.25 to 3.63V
- Recommended oscillation frequency range
 - (3rd overtone oscillator): 70 to 125MHz (2.5V±10%)
 - 75 to 135MHz (3.3V±10%)
- Output load 30pF (V_{DD} : 3.3V±10%, output frequency: 75 to 125MHz)
- Optimized oscillator circuit for large 3rd overtone crystal element with C_0 2 to 4pF
- -40 to 85°C operating temperature range
- CMOS output
- Output drive capability: ±8mA
- Standby function
 - High impedance in standby mode, oscillator stops
- Power-saving pull-up resistor built-in (INH pin)
- Wafer form (WF5056xx)
- Chip form (CF5056xx)

APPLICATIONS

- 7.0×5.0, 5.0×3.2 size crystal oscillator modules

SERIES CONFIGURATION

Version name*1	Recommended oscillation frequency range*2 [MHz]	Recommended C_0 value [pF]	Oscillator capacitance*3 [pF]	
			C_G	C_D
5056CC	70 to 85	$2 \leq C_0 \leq 4$	1	3
5056CE	100 to 135		0	1

*1. It becomes WF5056xx in case of the wafer form and CF5056xx in case of the chip form.

*2. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

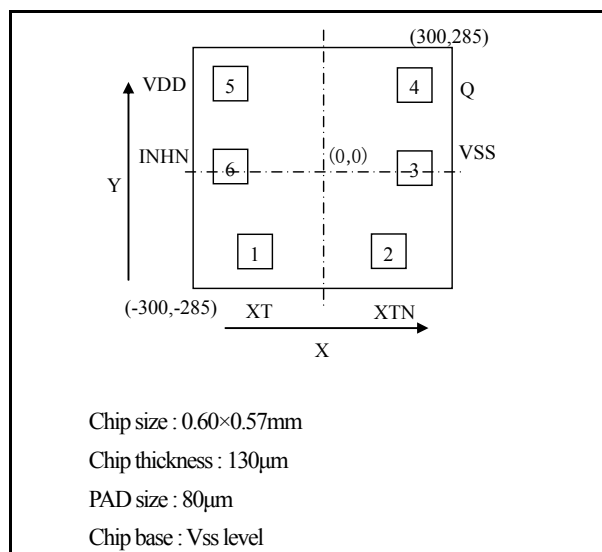
*3. The oscillator capacitance does not contain parasitic capacitance.

ORDERING INFORMATION

Device	Package	Version name
WF5056Cx-4	Wafer form	WF5056C□-4 Form WF : Wafer form ↑ CF : Chip(Die) form ↑ Oscillation frequency range ↑ PAD layout C: for Wire Bonding
CF5056Cx-4	Chip form	

PAD LAYOUT

(Unit: μm)



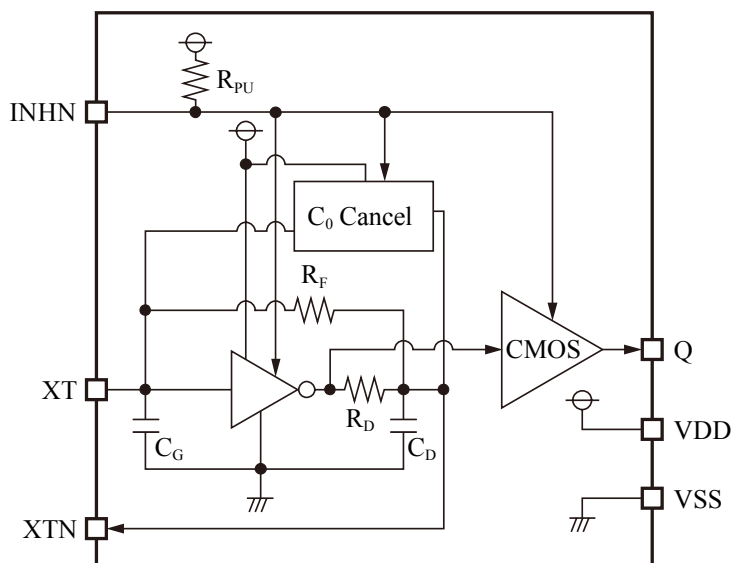
· Coordinates at the chip center are (0,0).

PIN DESCRIPTION and PAD COORDINATES

No.	Pin	I/O*1	Description	PAD coordinates [μm]	
				X	Y
1	XT	I	Crystal connection pins. Crystal is connected between XT and XTN.	-145.2	-193.5
2	XTN	O		145.2	-193.5
3	VSS	-	(-) ground	208.5	-1.1
4	Q	O	Output pin	208.5	193.5
5	VDD	-	(+) supply voltage	-208.5	193.5
6	INH	I	Input pin controlled output state (oscillator stops when LOW), Power-saving pull-up resistor built-in	-208.5	-1.1

*1. I: Input pin O: Output pin

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS}=0V$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range ^{*1}	V_{DD}	Between VDD and VSS	-0.3 to +4.0	V
Input voltage range ^{*1*2}	V_{IN}	Input pins	-0.3 to $V_{DD}+0.3$	V
Output voltage range ^{*1*2}	V_{OUT}	Output pins	-0.3 to $V_{DD}+0.3$	V
Output current ^{*3}	I_{OUT}	Q pin	± 20	mA
Junction temperature ^{*3}	T_j		125	°C
Storage temperature range ^{*4}	T_{STG}	Chip form, Wafer form	-55 to +125	°C

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded.

Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.

*2. V_{DD} is a V_{DD} value of recommended operating conditions.

*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.

*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

$V_{SS}=0V$

Parameter	Symbol	Condition	Rating			Unit		
			MIN	TYP	MAX			
Oscillator frequency ^{*1}	f_{OSC}	CC ver.	$V_{DD}=2.97$ to $3.63V$	75		85	MHz	
			$V_{DD}=2.25$ to $2.75V$	70		80		
		CE ver.	$V_{DD}=2.97$ to $3.63V$	100		135		
			$V_{DD}=2.25$ to $2.75V$	100		125		
Output frequency	f_{OUT}	CC ver.	$V_{DD}=2.97$ to $3.63V$ $C_{LOUT} \leq 30pF$	75		85	MHz	
			$V_{DD}=2.25$ to $2.75V$ $C_{LOUT} \leq 15pF$	70		80		
		CE ver.	$V_{DD}=2.97$ to $3.63V$	$C_{LOUT} \leq 15pF$	100		135	MHz
				$C_{LOUT} \leq 30pF$	100		125	
			$V_{DD}=2.25$ to $2.75V$	$C_{LOUT} \leq 15pF$	100		125	
				$C_{LOUT} \leq 15pF$	100		125	
Operating supply voltage	V_{DD}	Between VDD and V_{SS} ^{*2}	2.25		3.63	V		
Input voltage	V_{IN}	Input pins	V_{SS}		V_{DD}	V		
Operating temperature	T_a		-40		+85	°C		
Output load capacitance (Q pin)	C_{LOUT}	CC ver.	$V_{DD}=2.97$ to $3.63V$ and $75MHz \leq f_{OUT} \leq 85MHz$			30	pF	
		CE ver.	$V_{DD}=2.97$ to $3.63V$ and $100MHz \leq f_{OUT} \leq 125MHz$			30		
		Condition except the above				15		

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2. Mount a ceramic chip capacitor that is larger than $0.01\mu F$ proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5056 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics

DC Characteristics

$V_{DD}=2.25$ to 3.63 V, $V_{SS}=0$ V, $T_a=-40$ to $+85^{\circ}\text{C}$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit	
			MIN	TYP	MAX		
HIGH-level output voltage	V_{OH}	Q pin, measurement circuit 3, $I_{OH}=-8\text{mA}$	$V_{DD}-0.4$		V_{DD}	V	
LOW-level output voltage	V_{OL}	Q pin, measurement circuit 3, $I_{OL}=8\text{mA}$	0		0.4	V	
HIGH-level input voltage	V_{IH}	INH pin, measurement circuit 4	$0.7V_{DD}$			V	
LOW-level input voltage	V_{IL}	INH pin, measurement circuit 4			$0.3V_{DD}$	V	
Output leakage current	I_Z	Q pin, measurement circuit 5 INH="Low"	$Q=V_{DD}$		10	μA	
			$Q=V_{SS}$	-10			
Current consumption*1	CC ver.	$I_{DD,3.3V}$ $I_{DD,2.5V}$	Measurement circuit 1, no load INH="OPEN", $f_{OSC}=80\text{MHz}$	$V_{DD}=3.3\text{V}$	15	30	mA
				$V_{DD}=2.5\text{V}$	8	16	
	CE ver.	$I_{DD,3.3V}$ $I_{DD,2.5V}$	Measurement circuit 1, no load INH="OPEN", $f_{OSC}=125\text{MHz}$	$V_{DD}=3.3\text{V}$	17	34	
				$V_{DD}=2.5\text{V}$	10	20	
Standby current	I_{ST}	Measurement circuit 1, INH= V_{SS}			10	μA	
INH pull-up resistance		R_{PU1}	Measurement circuit 6	0.8	3	24	$\text{M}\Omega$
		R_{PU2}	Measurement circuit 6	30	70	150	$\text{k}\Omega$
Oscillator feedback resistance	CC ver.	R_f	Design value	2.7	4.9	7.1	$\text{k}\Omega$
	CE ver.	R_f	Design value	2.0	3.8	5.5	
Oscillator capacitance	CC ver.	C_G	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	0.8	1	1.2	pF
		C_D		2.4	3	3.6	
	CE ver.	C_G	Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance.	0	0	0	pF
		C_D		0.8	1	1.2	

*1. The consumption current $I_{DD}(C_{LOUT})$ with a load capacitance(C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.

$$I_{DD}(C_{LOUT})[\text{mA}] = I_{DD}[\text{mA}] + C_{LOUT}[\text{pF}] \times V_{DD}[\text{V}] \times f_{OUT}[\text{MHz}] \cdot 10^{-3}$$

AC Characteristics

$V_{DD}=2.25$ to 3.63 V, $V_{SS}=0$ V, $T_a=-40$ to $+85^\circ\text{C}$ unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			MIN	TYP	MAX	
Output rise time	t_{r1}	Measurement circuit 1, $C_{LOUT}=15\text{pF}$, $0.1V_{DD} \rightarrow 0.9V_{DD}$, $V_{DD}=2.25$ to 3.63 V		1.0	2.0	ns
	t_{r2}	Measurement circuit 1, $C_{LOUT}=30\text{pF}$, $0.1V_{DD} \rightarrow 0.9V_{DD}$, $V_{DD}=2.97$ to 3.63 V		1.5	2.5	
Output fall time	t_{f1}	Measurement circuit 1, $C_{LOUT}=15\text{pF}$, $0.9V_{DD} \rightarrow 0.1V_{DD}$, $V_{DD}=2.25$ to 3.63 V		1.0	2.0	ns
	t_{f2}	Measurement circuit 1, $C_{LOUT}=30\text{pF}$, $0.9V_{DD} \rightarrow 0.1V_{DD}$, $V_{DD}=2.97$ to 3.63 V		1.5	3.0	
Output duty cycle	DUTY	Measurement circuit 1, $T_a=25^\circ\text{C}$, $C_{LOUT}=15\text{pF}$, $V_{DD}=2.25$ to 3.63 V	45	50	55	%
		Measurement circuit 1, $T_a=25^\circ\text{C}$, $C_{LOUT}=30\text{pF}$, $V_{DD}=2.97$ to 3.63 V	40	50	60	
Output disable delay time	t_{OD}	Measurement circuit 2, $T_a=25^\circ\text{C}$, $C_{LOUT}\leq 15\text{pF}$			200	ns

Note. The ratings above are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated.

Timing chart

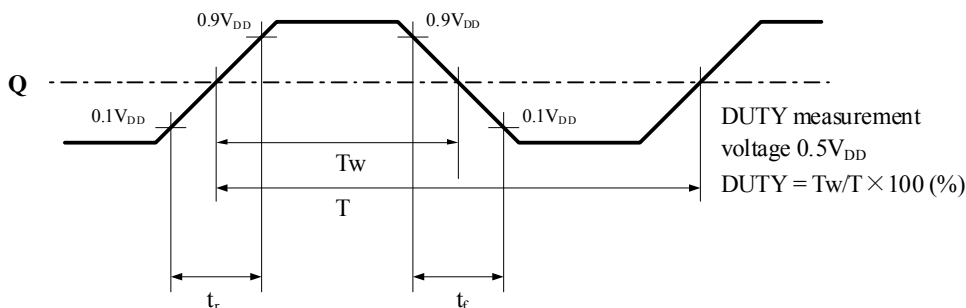
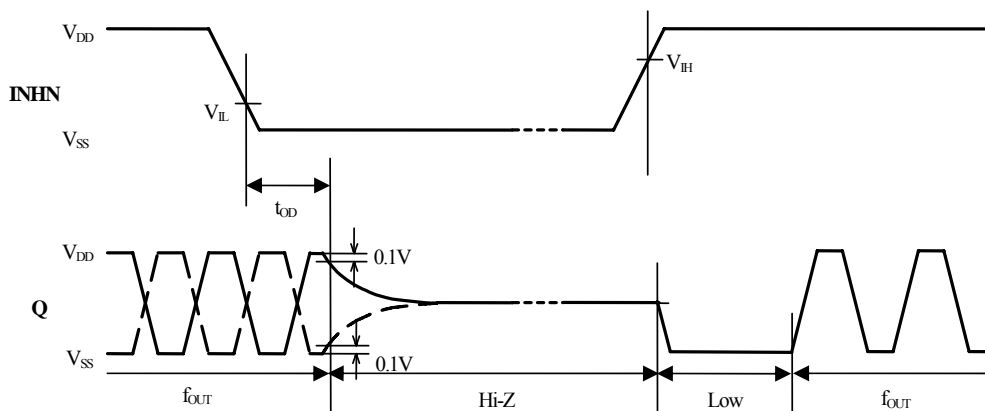


Figure 1. Output switching waveform



When INHN goes HIGH to LOW, the Q output becomes high impedance.

When INHN goes LOW to HIGH, the Q output goes LOW once and then becomes normal output operation after having detected oscillation signals.

Figure 2. Output disable and oscillation start timing chart

FUNCTIONAL DESCRIPTION

Standby Function

When INHN goes LOW level, the Q output becomes high impedance.

INHN	Q	Oscillator
HIGH(Open)	f_{OUT}	Operating
LOW	Hi-Z	Stopped

Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to R_{PU1} or R_{PU2} in response to the input level (HIGH or LOW).

When INHN is tied to LOW level, the pull-up resistance becomes large (R_{PU1}), thus reducing the current consumed by the resistance.

When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small (R_{PU2}), thus internal circuit of INHN becomes HIGH level. Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

Oscillation Detection Function

The 5056 series incorporate an oscillation detection circuit. The oscillation detection circuit disables the output until the oscillator circuit starts up. This function avoids the problem where the oscillator does not start, due to abnormal oscillation conditions, where power is applied or when the oscillator is restarted using INHN.

C_0 cancellation circuit

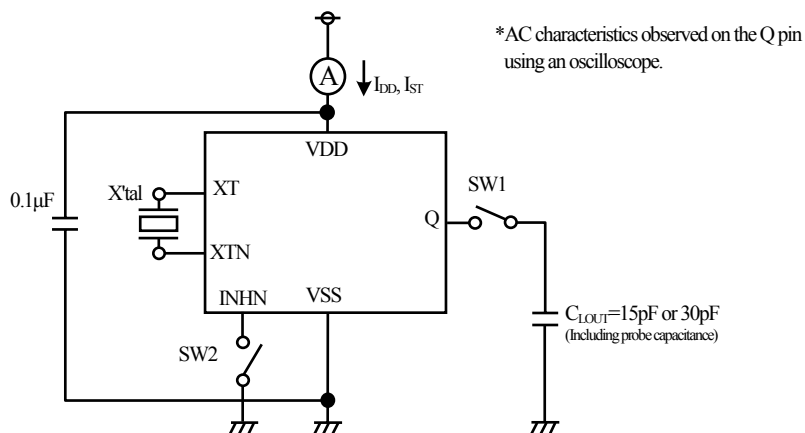
Oscillation circuit with a built-in C_0 cancellation circuit provides a fixed compensation amount to cancel the effect of the crystal C_0 . It reduces the C_0 parameter in the equivalent circuit, reducing the shallow negative resistance for increasing values of C_0 .

This cancellation circuit makes it easier to maintain the oscillation margin.

MEASUREMENT CIRCUITS

MEASUREMENT CIRCUIT 1

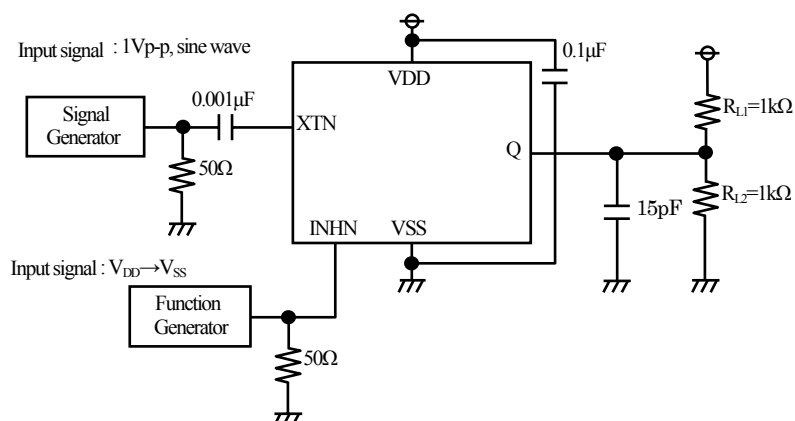
Measurement Parameter: I_{DD} , I_{ST} , DUTY, t_s , t_f



Parameter	SW1	SW2
I_{DD}	OFF	OFF
I_{ST}	ON or OFF	ON
DUTY, t_s , t_f	ON	OFF

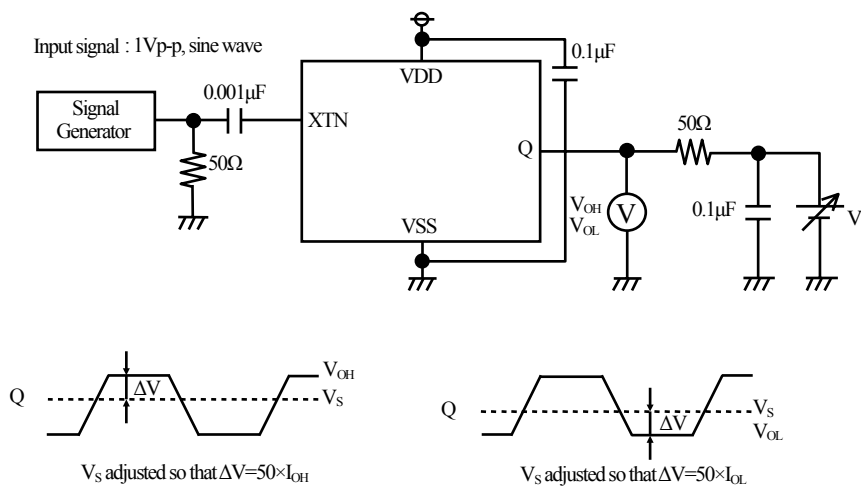
MEASUREMENT CIRCUIT 2

Measurement Parameter: t_{OD}



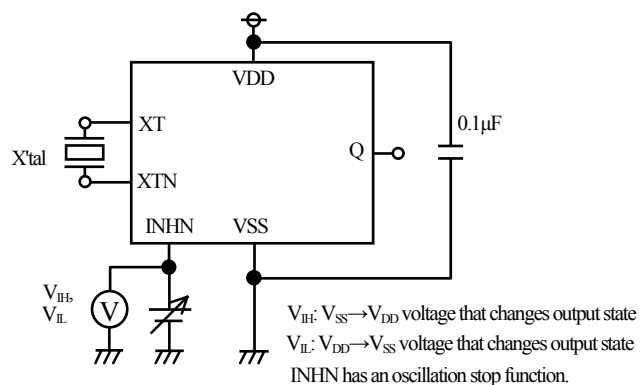
MEASUREMENT CIRCUIT 3

Measurement Parameter: V_{OH} , V_{OL}



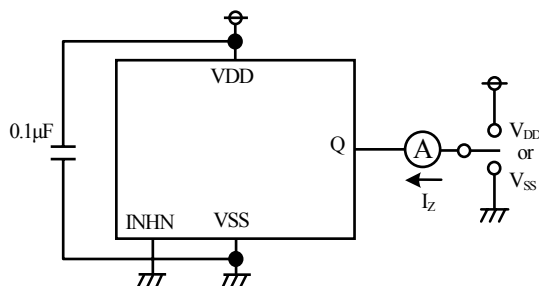
MEASUREMENT CIRCUIT 4

Measurement Parameter: V_{IH} , V_{IL}



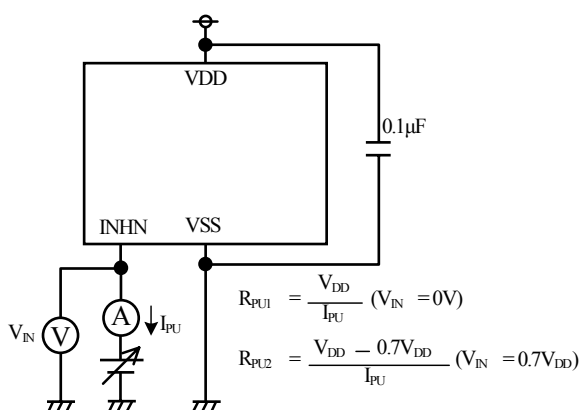
MEASUREMENT CIRCUIT 5

Measurement Parameter: I_Z



MEASUREMENT CIRCUIT 6

Measurement Parameter: R_{PU1} , R_{PU2}



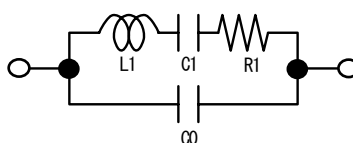
REFERENCE DATA

The following characteristics are measured using the crystal below. Note that the characteristics will vary with the crystal used.

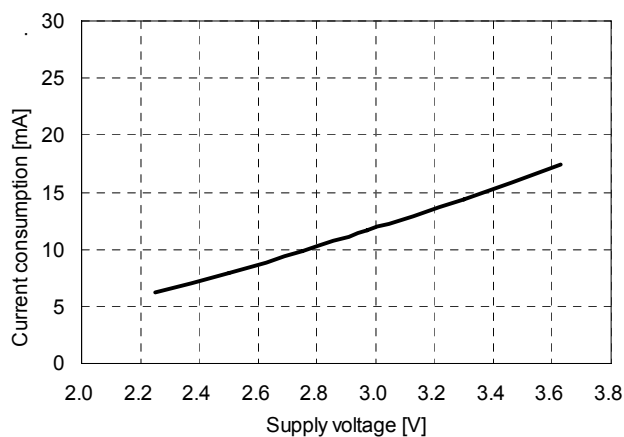
Crystal used for measurement

Parameter	80MHz	125MHz
C_0 (pF)	2.4	2.0
R_1 (Ω)	42	33

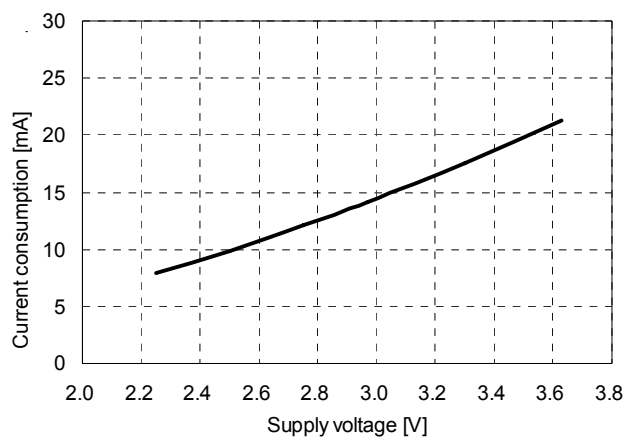
Crystal parameters



Current Consumption

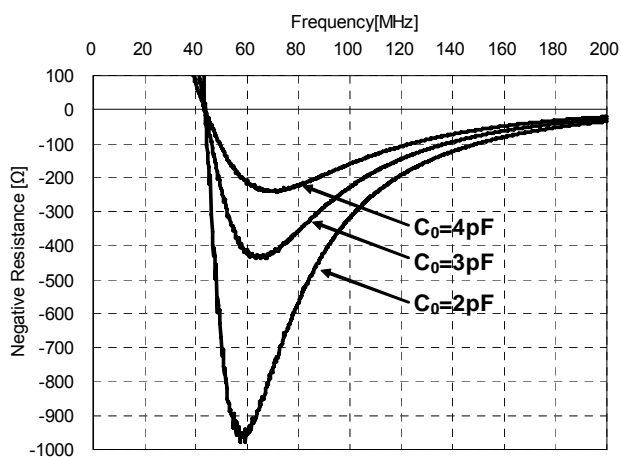


5056CC, $f_{osc}=80\text{MHz}$, $T_a=25^\circ\text{C}$, no load

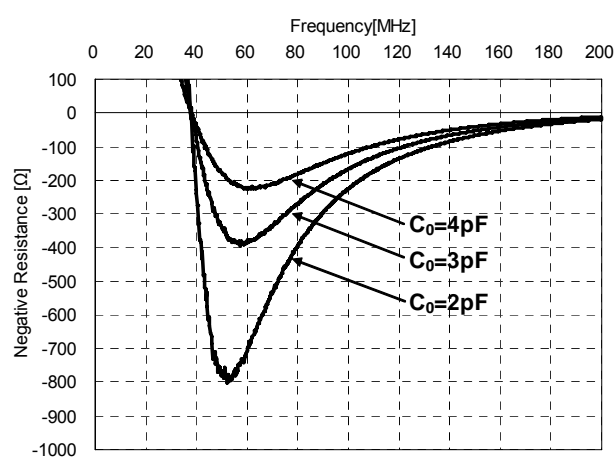


5056CE, $f_{osc}=125\text{MHz}$, $T_a=25^\circ\text{C}$, no load

Negative Resistance

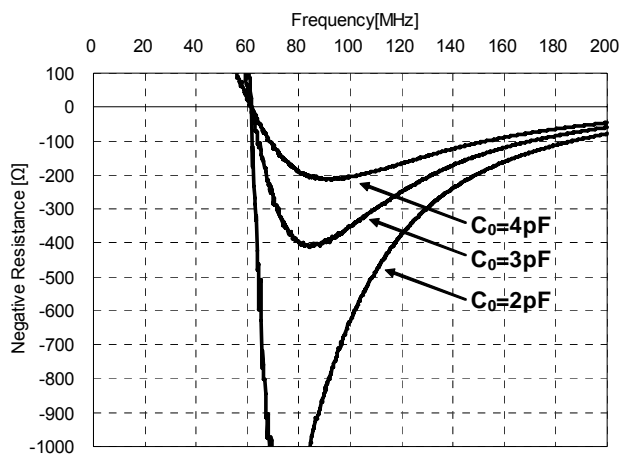


5056CC, $V_{DD}=3.3\text{V}$, $T_a=25^\circ\text{C}$

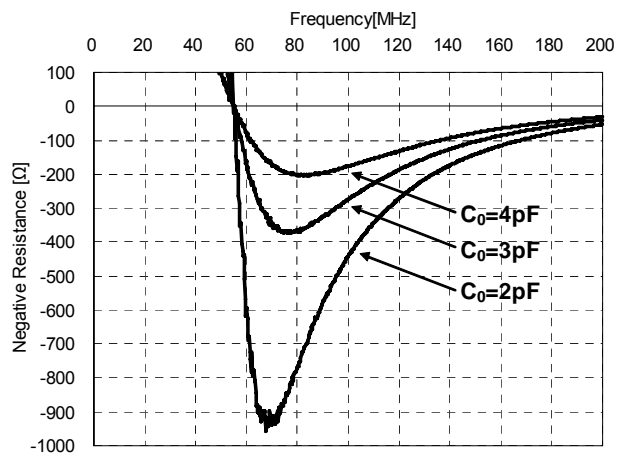


5056CC, $V_{DD}=2.5\text{V}$, $T_a=25^\circ\text{C}$

5056 series



5056CE, $V_{DD}=3.3V$, $T_a=25^\circ C$

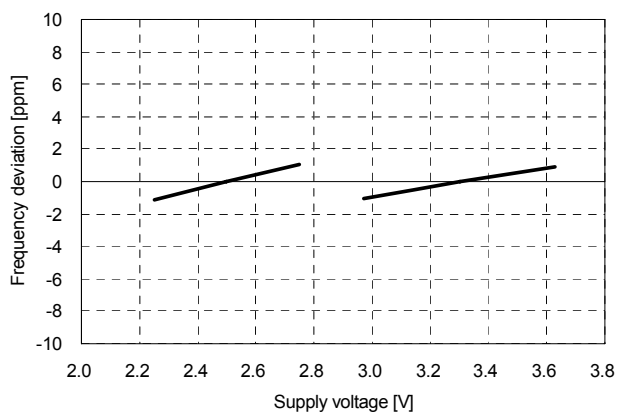


5056CE, $V_{DD}=2.5V$, $T_a=25^\circ C$

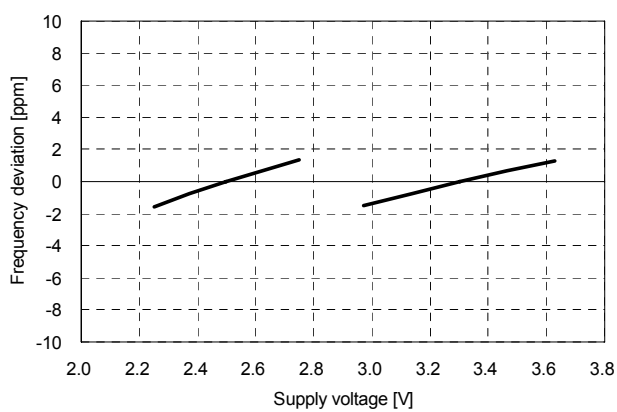
Measurement equipment: Agilent 4396B Impedance Analyzer

The figures show the measurement result of the crystal equivalent circuit C_0 capacitance, connected between the XT and XTN pins. They were performed with Agilent 4396B using the NPC test jig. They may vary in a measurement jig, and measurement environment.

Frequency Deviation by Voltage



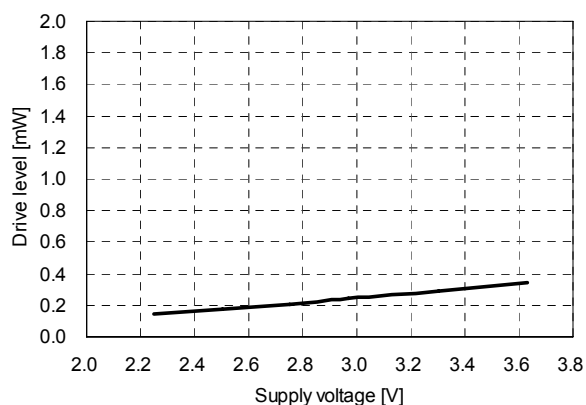
5056CC, $f_{OSC}=80MHz$, $T_a=25^\circ C$, 2.5V and 3.3V std.



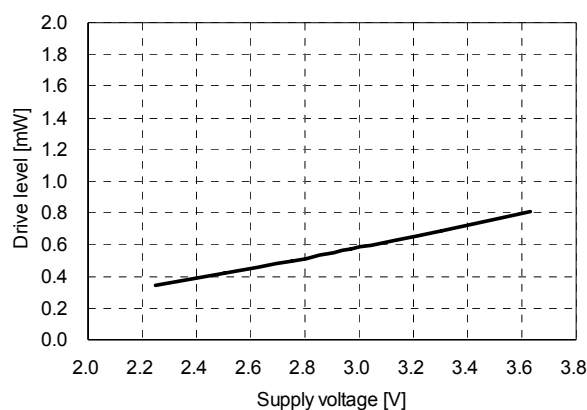
5056CE, $f_{OSC}=125MHz$, $T_a=25^\circ C$, 2.5V and 3.3V std.

Measurement equipment: Agilent 53132A Frequency Counter

Drive Level



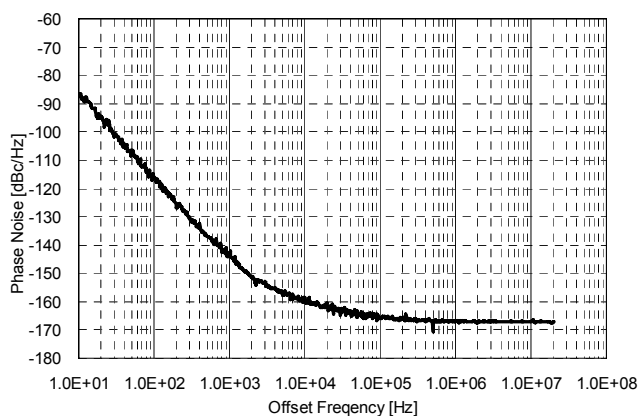
5056CC, $f_{osc}=80\text{MHz}$, $T_a=25^\circ\text{C}$



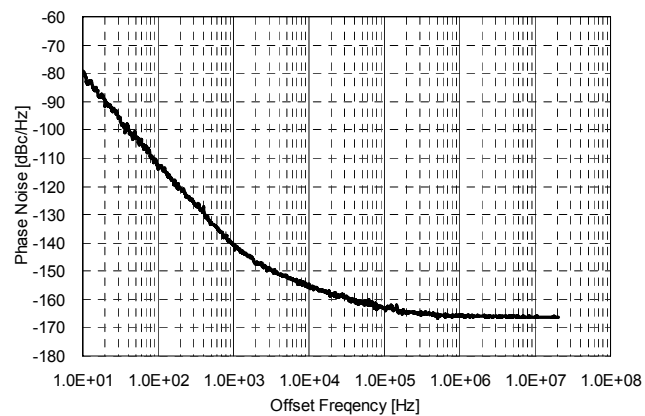
5056CE, $f_{osc}=125\text{MHz}$, $T_a=25^\circ\text{C}$

Measurement equipment: Agilent DSO80604B Digital Oscilloscope
 Tektronix CT-6 Current probe
 Agilent 53132A Frequency Counter

Phase Noise



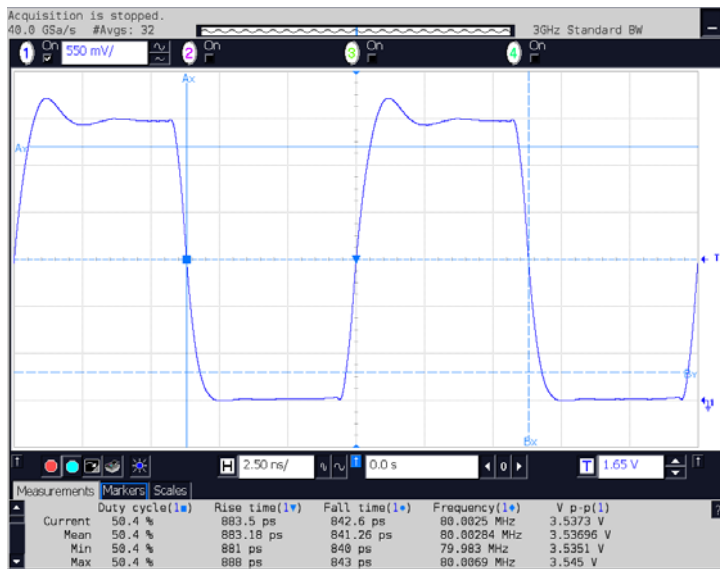
5056CC, $V_{DD}=3.3\text{V}$, $f_{osc}=80\text{MHz}$, $T_a=25^\circ\text{C}$



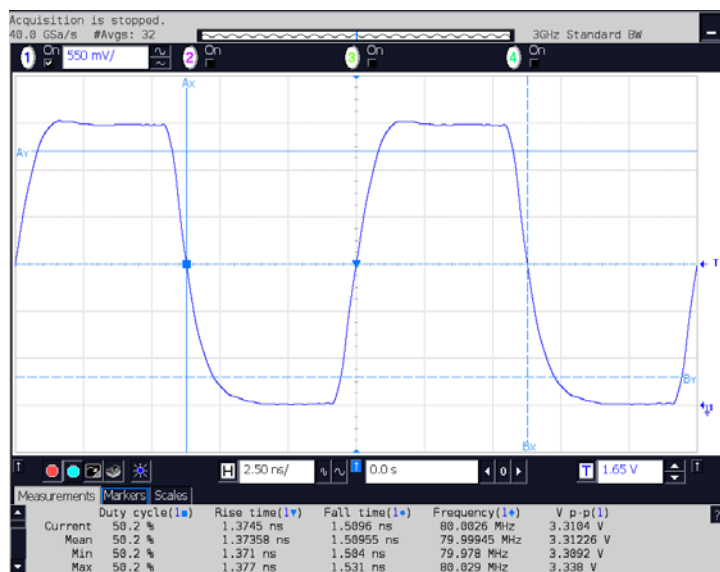
5056CE, $V_{DD}=3.3\text{V}$, $f_{osc}=125\text{MHz}$, $T_a=25^\circ\text{C}$

Measurement equipment: Signal Source Analyzer Agilent E5052B

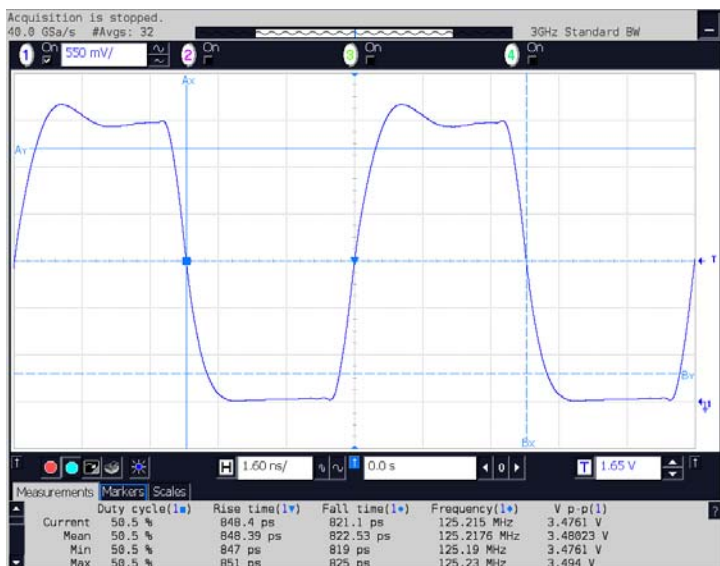
Output Waveform



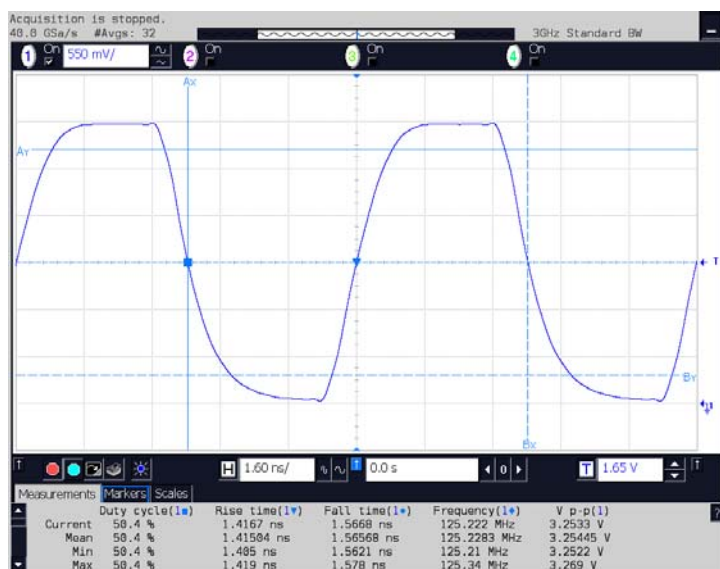
5056CC, $V_{DD}=3.3V$, $f_{osc}=80MHz$, $T_a=25^{\circ}C$, $C_{LOUT}=15pF$



5056CC, $V_{DD}=3.3V$, $f_{osc}=80MHz$, $T_a=25^{\circ}C$, $C_{LOUT}=30pF$



5056CE, $V_{DD}=3.3V$, $f_{OSC}=125MHz$, $T_a=25^{\circ}C$, $C_{LOUT}=15pF$



5056CE, $V_{DD}=3.3V$, $f_{OSC}=125MHz$, $T_a=25^{\circ}C$, $C_{LOUT}=30pF$

Measurement equipment: Oscilloscope Agilent DSO80604B
 Differential probe 1134A (Probe head E2678A)

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The logo for NPC (Seiko NPC Corporation) consists of the letters 'NPC' in a bold, black, sans-serif font. The 'N' and 'P' are connected at the top, and the 'C' is positioned to the right of the 'P'.

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