OVERVIEW
The 5078 series are CMOS output VCXO ICs that provide a wide frequency pulling range. They employ bipolar oscillator circuit and recently developed varicap diode fabrication process that provides a low phase noise characteristic and a wide frequency pulling range without any external components. The 5078 series are ideal for wide pulling range, low phase noise, VCXO modules.

FEATURES
- VCXO with recently developed varicap diode built-in
- Oscillator: Fundamental frequency oscillation
- Output frequency: 30 to 170MHz
- Operating supply voltage range: 2.97 to 3.63V
- Oscillator frequency range (for fundamental oscillation):
  - 60 to 100MHz (Ax version)
  - 100 to 170MHz (Bx version)
- Frequency pulling range:
  - ±150ppm@A1 version, $V_{C}=1.65±1.65V$, $f=77.76MHz$ ($γ=290$, $C_0=2.4pF$)
  - ±130ppm@B1 version, $V_{C}=1.65±1.65V$, $f=155.52MHz$ ($γ=330$, $C_0=1.5pF$)
- Low phase noise:
  - -130dBc/Hz@A1 version, 1kHz Offset, $f=77.76MHz$ ($γ=290$, $C_0=2.4pF$)
  - -162dBc/Hz@A1 version, 10MHz Offset, $f=77.76MHz$
  - -125dBc/Hz@B1 version, 1kHz Offset, $f=155.52MHz$ ($γ=330$, $C_0=1.5pF$)
  - -162dBc/Hz@B1 version, 10kHz Offset, $f=155.52MHz$

APPLICATIONS
SONET/SDH, Ethernet, Fibre Channel, LTE

SERIES CONFIGURATION

<table>
<thead>
<tr>
<th>Version Name</th>
<th>Recommended operating frequency range ($f_{osc}$)/[MHz]</th>
<th>Output frequency ($f_{out}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5078A1</td>
<td>60MHz to 100MHz</td>
<td>$f_{osc}$</td>
</tr>
<tr>
<td>5078A2</td>
<td>60MHz to 100MHz</td>
<td>$f_{osc}/2$</td>
</tr>
<tr>
<td>5078B1</td>
<td>100MHz to 170MHz</td>
<td>$f_{osc}$</td>
</tr>
<tr>
<td>5078B2</td>
<td>100MHz to 170MHz</td>
<td>$f_{osc}/2$</td>
</tr>
</tbody>
</table>

*1. The recommended oscillation frequency is a yardstick value derived from the resonator used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to resonator characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

The recommended characteristics for the crystal element are:
- A versions: $R_1 < 20Ω$, $C_0 < 1.5pF$
- B versions: $R_1 < 20Ω$, $C_0 < 1.5pF$

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Version name</th>
</tr>
</thead>
<tbody>
<tr>
<td>WF5078xx-4</td>
<td>Wafer form</td>
<td>WF5078□□-4</td>
</tr>
<tr>
<td>CF5078xx-4</td>
<td>Chip form</td>
<td></td>
</tr>
</tbody>
</table>

Form WF: Wafer form
CF: Chip(Die) form
Frequency divider function
Oscillation frequency range
5078 series

PAD LAYOUT
(Unit: μm)

Chip size: 0.9mm×0.9mm
Chip thickness: 130μm
PAD size: 80μm×80μm (PAD No.1, 2, 3, 4, 6, 7 pins)
80μm×160μm (PAD No.5 pin)
Chip base: VSS potential

PAD LAYOUT

PIN DESCRIPTION and PAD COORDINATES

<table>
<thead>
<tr>
<th>No.</th>
<th>Pin</th>
<th>I/O</th>
<th>Description</th>
<th>Pad Coordinates (Unit : μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>XT</td>
<td>I</td>
<td>Crystal connection pin</td>
<td>X</td>
</tr>
<tr>
<td>2</td>
<td>XTN</td>
<td>O</td>
<td>Crystal connection pin</td>
<td>-345.0</td>
</tr>
<tr>
<td>3</td>
<td>VC</td>
<td>I</td>
<td>Control voltage input pin</td>
<td>-75.4</td>
</tr>
<tr>
<td>4</td>
<td>INHN</td>
<td>I</td>
<td>Input pin controlled output state(oscillator stops when LOW),</td>
<td>93.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Power-saving pull-up resistor built-in</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>VSS</td>
<td>-</td>
<td>(-) ground</td>
<td>337.0</td>
</tr>
<tr>
<td>6</td>
<td>Q</td>
<td>O</td>
<td>Output one of fOSC, fOSC/2</td>
<td>331.9</td>
</tr>
<tr>
<td>7</td>
<td>VDD</td>
<td>-</td>
<td>(+) supply voltage</td>
<td>50.1</td>
</tr>
</tbody>
</table>

*1. I: Input pin  O: Output pin
BLOCK DIAGRAM

INHN

XT

XTN

VC

VDD

R_{pu1}, R_{pu2}

\frac{1}{N}

Level Shifter

Divider CMOS

N=1,2 (Mask Option)

\begin{align*}
\text{OSC} & \quad \rightarrow \\
\text{Level Shifter} & \quad \rightarrow \\
\text{1/N Divider} & \quad \rightarrow \\
\text{CMOS} & \quad \rightarrow \\
Q & \quad \rightarrow \\
\text{VSS} & \quad \rightarrow
\end{align*}
SPECIFICATIONS

Absolute Maximum Ratings

\( V_{\text{SS}} = 0\text{V} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage range*1</td>
<td>( V_{\text{DD}} )</td>
<td>VDD pin</td>
<td>(-0.3 \text{ to } +5.0)</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage range*2</td>
<td>( V_{\text{IN}} )</td>
<td>Input pins</td>
<td>(-0.3 \text{ to } V_{\text{DD}} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage range*2</td>
<td>( V_{\text{OUT}} )</td>
<td>Output pins</td>
<td>(-0.3 \text{ to } V_{\text{DD}} + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>Junction temperature*3</td>
<td>( T_{j} )</td>
<td></td>
<td>(+125)</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range*4</td>
<td>( T_{\text{STG}} )</td>
<td>Wafer, Chip form</td>
<td>(-55 \text{ to } +125)</td>
<td>°C</td>
</tr>
<tr>
<td>Output current*3</td>
<td>( I_{\text{OUT}} )</td>
<td>Q pin</td>
<td>( T_{a} = -40 \text{ to } +85)</td>
<td>±20 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( T_{a} = -40 \text{ to } +105)</td>
<td>±10 mA</td>
</tr>
</tbody>
</table>

*1. This parameter rating is the values that must never exceed even for a moment. This product may suffer breakdown if this parameter rating is exceeded.
Operation and characteristics are guaranteed only when the product is operated at recommended operating conditions.

*2. \( V_{\text{DD}} \) is a \( V_{\text{DD}} \) value of recommended operating conditions.

*3. Do not exceed the absolute maximum ratings. If they are exceeded, a characteristic and reliability will be degraded.

*4. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

\( V_{\text{SS}} = 0\text{V} \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating supply voltage</td>
<td>( V_{\text{DD}} )</td>
<td>Between VDD and VSS pins*2</td>
<td>( 2.97 \text{ to } 3.63)</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage</td>
<td>( V_{\text{IN}} )</td>
<td>INHN, VC pins</td>
<td>( 0 \text{ to } V_{\text{DD}})</td>
<td>V</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>( T_{a} )</td>
<td>-40 to +105</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Output load capacitance</td>
<td>( C_{L} )</td>
<td></td>
<td>15</td>
<td>pF</td>
</tr>
<tr>
<td>Oscillator frequency range*1</td>
<td>( f_{\text{OSC}} )</td>
<td>5078Ax</td>
<td>( 60 \text{ to } 100)</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5078Bx</td>
<td>100</td>
<td>170</td>
</tr>
<tr>
<td>Output frequency range</td>
<td>( f_{\text{OUT}} )</td>
<td>5078A1</td>
<td>( 60 \text{ to } 100)</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5078A2</td>
<td>30</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5078B1</td>
<td>100</td>
<td>170</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5078B2</td>
<td>50</td>
<td>85</td>
</tr>
</tbody>
</table>

*1. The oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*2. Mount a ceramic chip capacitor that is larger than 0.01 \( \mu \text{F} \) proximal to IC (within approximately 3mm) between VDD and VSS in order to obtain stable operation of 5078 series. In addition, the wiring pattern between IC and capacitor should be as wide as possible.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.
## Electrical Characteristics

### A1, A2 version

\( V_{DD} = 2.97 \text{ to } 3.63 \text{V}, \quad V_C = 0.5 \text{V}_{DD}, \quad V_{SS} = 0 \text{V}, \quad T_a = -40 \text{ to } +105^\circ \text{C} \) unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption</td>
<td>( I_{DD} )</td>
<td>measurement circuit 1, no load, INHN=Open ( V_{DD}=3.3 \text{V}, f_{OSC}=77.76 \text{MHz}, f_{OUT}=77.76 \text{MHz} )</td>
<td>5.2</td>
<td>8.0 mA</td>
</tr>
<tr>
<td>A1 version: ( f_{OSC} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current consumption</td>
<td>( I_{DD} )</td>
<td>measurement circuit 1, no load, INHN=Open ( V_{DD}=3.3 \text{V}, f_{OSC}=38.88 \text{MHz} )</td>
<td>4.2</td>
<td>7.0 mA</td>
</tr>
<tr>
<td>A2 version: ( f_{OSC}/2 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standby current</td>
<td>( I_{STB} )</td>
<td>measurement circuit 1, INHN=0V ( T_a=-40 \text{ to } +85^\circ \text{C} )</td>
<td>10</td>
<td>100 μA</td>
</tr>
<tr>
<td>High-level output voltage</td>
<td>( V_{OH} )</td>
<td>measurement circuit 2, Q pin, ( I_{OH}=-4 \text{mA} ) ( V_{DD}=0.4 \text{V} )</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Low-level output voltage</td>
<td>( V_{OL} )</td>
<td>measurement circuit 2, Q pin, ( I_{OL}=4 \text{mA} ) ( V_{DD}=0.4 \text{V} )</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>Output leakage current</td>
<td>( I_{L} )</td>
<td>measurement circuit 3, Q pin, INHN=0V, ( T_a=25^\circ \text{C} )</td>
<td>-1</td>
<td>1 μA</td>
</tr>
<tr>
<td>High-level input voltage</td>
<td>( V_{IH} )</td>
<td>measurement circuit 4, INHN pin ( V_{DD}=0.7 \text{V} )</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>Low-level input voltage</td>
<td>( V_{IL} )</td>
<td>measurement circuit 4, INHN pin ( V_{DD}=0.3 \text{V} )</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>Pull-up resistance 1</td>
<td>( R_{PUI} )</td>
<td>measurement circuit 5, INHN pin, INHN=0V</td>
<td>1</td>
<td>9 MΩ</td>
</tr>
<tr>
<td>Pull-up resistance 2</td>
<td>( R_{PUL2} )</td>
<td>measurement circuit 5, INHN pin, INHN=0.7V</td>
<td>50</td>
<td>200 kΩ</td>
</tr>
<tr>
<td>Oscillator block built-in resistance*1</td>
<td>( R_{VC1} )</td>
<td>measurement circuit 6, between VC and XT</td>
<td>100</td>
<td>300 kΩ</td>
</tr>
<tr>
<td></td>
<td>( R_{VC2} )</td>
<td>measurement circuit 6, between VC and XTN</td>
<td>100</td>
<td>300 kΩ</td>
</tr>
<tr>
<td>Input leakage resistance*1</td>
<td>( R_{VIN} )</td>
<td>measurement circuit 7, VC pin, ( T_a=25^\circ \text{C} )</td>
<td>10</td>
<td>MΩ</td>
</tr>
<tr>
<td>Oscillator block built-in capacitance</td>
<td>( C_{VC1} )</td>
<td>Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance. ( V_{C}=0.3 \text{V} )</td>
<td>5.88</td>
<td>7.18 pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{C}=1.65 \text{V} )</td>
<td>3.51</td>
<td>4.75 pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{C}=3.0 \text{V} )</td>
<td>1.80</td>
<td>2.70 pF</td>
</tr>
<tr>
<td></td>
<td>( C_{VC2} )</td>
<td>Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance. ( V_{C}=0.3 \text{V} )</td>
<td>8.82</td>
<td>10.78 pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{C}=1.65 \text{V} )</td>
<td>5.27</td>
<td>7.13 pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{C}=3.0 \text{V} )</td>
<td>2.70</td>
<td>4.06 pF</td>
</tr>
<tr>
<td>Maximum modulation frequency</td>
<td>( F_M )</td>
<td>-3dB frequency, ( T_a=25^\circ \text{C} ) ( V_{DD}=3.3 \text{V}, V_{C}=1.65\pm1.65 \text{V} )</td>
<td>20</td>
<td>50 kHz</td>
</tr>
</tbody>
</table>

*1. These prescriptions indicate the following contents:
   Oscillator block built-in resistance: Resistance between VC - XT or XTN
   Input leakage resistance: Resistance between VC - VSS (DC characteristic)
   Refer to pg.22 for VC Terminal Input Impedance.
**B1, B2 version**

\[ V_{DD}=2.97 \text{ to } 3.63V, V_C=0.5V_{DD}, V_{SS}=0V, T_a=-40 \text{ to } +105^\circ C \text{ unless otherwise noted.} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption</td>
<td>( I_{DD} )</td>
<td>measurement circuit 1, no load, INHN=Open ( V_{DD}=3.3V, f_{OSC}=155.52MHz, f_{OUT}=155.52MHz )</td>
<td>MIN 10 TYP 15 MAX mA</td>
<td></td>
</tr>
<tr>
<td>Current consumption</td>
<td>( I_{DD} )</td>
<td>measurement circuit 1, no load, INHN=Open ( V_{DD}=3.3V, f_{OSC}=155.52MHz, f_{OUT}=77.76MHz )</td>
<td>MIN 8.1 TYP 12 MAX mA</td>
<td></td>
</tr>
<tr>
<td>Standby current</td>
<td>( I_{STB} )</td>
<td>measurement circuit 1, INHN=0V ( T_a=-40 \text{ to } +85^\circ C )</td>
<td>MIN 10 TYP 100 MAX ( \mu A )</td>
<td></td>
</tr>
<tr>
<td>High-level output voltage</td>
<td>( V_{OH} )</td>
<td>measurement circuit 2, Q pin, ( I_{OH}=-8mA ) ( V_{DD}=0.4V )</td>
<td>0.7V_{DD} V</td>
<td></td>
</tr>
<tr>
<td>Low-level output voltage</td>
<td>( V_{OL} )</td>
<td>measurement circuit 2, Q pin, ( I_{OH}=8mA )</td>
<td>0.4 V</td>
<td></td>
</tr>
<tr>
<td>Output leakage current</td>
<td>( I_{Z} )</td>
<td>measurement circuit 3, Q pin, INHN=0V ( T_a=25^\circ C )</td>
<td>MIN -1 TYP 1 MAX ( \mu A )</td>
<td></td>
</tr>
<tr>
<td>High-level input voltage</td>
<td>( V_{IH} )</td>
<td>measurement circuit 4, INHN pin ( V_{C} )</td>
<td>0.7V_{DD} V</td>
<td></td>
</tr>
<tr>
<td>Low-level input voltage</td>
<td>( V_{IL} )</td>
<td>measurement circuit 4, INHN pin ( V_{C} )</td>
<td>0.3V_{DD} V</td>
<td></td>
</tr>
<tr>
<td>Pull-up resistance 1</td>
<td>( R_{PU1} )</td>
<td>measurement circuit 5, INHN pin, INHN=0V ( V_{C} )</td>
<td>MIN 1 TYP 4 MAX 9 k\Omega</td>
<td></td>
</tr>
<tr>
<td>Pull-up resistance 2</td>
<td>( R_{PU2} )</td>
<td>measurement circuit 5, INHN pin, INHN=0.7V_{DD} ( V_{C} )</td>
<td>MIN 50 TYP 100 MAX 200 k\Omega</td>
<td></td>
</tr>
<tr>
<td>Oscillator block built-in resistance*1</td>
<td>( R_{VC1} )</td>
<td>measurement circuit 6, between VC and XT ( V_{C} )</td>
<td>MIN 100 TYP 200 MAX 300 k\Omega</td>
<td></td>
</tr>
<tr>
<td>Oscillator block built-in resistance*1</td>
<td>( R_{VC2} )</td>
<td>measurement circuit 6, between VC and XTN ( V_{C} )</td>
<td>MIN 100 TYP 200 MAX 300 k\Omega</td>
<td></td>
</tr>
<tr>
<td>Input leakage resistance*1</td>
<td>( R_{VIN} )</td>
<td>measurement circuit 7, VC pin, ( T_a=25^\circ C ) ( V_{C} )</td>
<td>MIN 10 MAX M\Omega</td>
<td></td>
</tr>
<tr>
<td>Oscillator block built-in capacitance</td>
<td>( C_{VC1} )</td>
<td>Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance. ( V_{C}=0.3V )</td>
<td>4.38 4.86 5.35 pF</td>
<td></td>
</tr>
<tr>
<td>Oscillator block built-in capacitance</td>
<td>( C_{VC2} )</td>
<td>Design value (a monitor pattern on a wafer is tested), Excluding parasitic capacitance. ( V_{C}=0.3V )</td>
<td>6.24 6.94 7.63 pF</td>
<td></td>
</tr>
<tr>
<td>Maximum modulation frequency</td>
<td>( F_M )</td>
<td>-3dB frequency, ( T_a=25^\circ C ) ( V_{DD}=3.3V, V_C=1.65V \pm 1.65V ) ( V_{DD}=3.3V, f_{OSC}=155.52MHz )</td>
<td>MIN 20 TYP 50 MAX kHz</td>
<td></td>
</tr>
</tbody>
</table>

*1. These prescriptions indicate the following contents.
Oscillator block built-in resistance: Resistance between VC - XT or XTN
Input leakage resistance: Resistance between VC - VSS (DC characteristic)
Refer to pg.22 for VC Terminal Input Impedance.
Switching Characteristics
A1, A2 version

\[ V_{DD} = 2.97 \text{ to } 3.63V, \ V_C = 0.5V_{DD}, \ V_{SS} = 0V, \ T_a = -40 \text{ to } +105^\circ C \text{ unless otherwise noted} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC “H” level output voltage</td>
<td>( V_{\text{TOP}} )</td>
<td>measurement circuit 9, ( C_L = 15pF )</td>
<td>0.9( V_{DD} )</td>
<td>V</td>
</tr>
<tr>
<td>AC “L” level output voltage</td>
<td>( V_{\text{BASE}} )</td>
<td>measurement circuit 9, ( C_L = 15pF )</td>
<td>0.1( V_{DD} )</td>
<td>V</td>
</tr>
<tr>
<td>Duty cycle</td>
<td>Duty</td>
<td>measurement circuit 9, ( T_a = 25^\circ C, \ V_{DD} = 3.3V )</td>
<td>45</td>
<td>55</td>
</tr>
<tr>
<td>Output rise time</td>
<td>( t_r )</td>
<td>measurement circuit 9, ( C_L = 15pF, 0.1V_{DD} \rightarrow 0.9V_{DD} )</td>
<td>1.5</td>
<td>3.0</td>
</tr>
<tr>
<td>Output fall time</td>
<td>( t_f )</td>
<td>measurement circuit 9, ( C_L = 15pF, 0.9V_{DD} \rightarrow 0.1V_{DD} )</td>
<td>1.5</td>
<td>3.0</td>
</tr>
<tr>
<td>Output enable propagation delay</td>
<td>( t_{OE} )</td>
<td>measurement circuit 10, ( T_a = 25^\circ C ) INHN= “Low” \rightarrow “High” \</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Output disable propagation delay</td>
<td>( t_{OD} )</td>
<td>measurement circuit 10, ( T_a = 25^\circ C ) INHN= “High” \rightarrow “Low” \</td>
<td>200</td>
<td></td>
</tr>
</tbody>
</table>

Note: The ratings are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated. The recommended crystal element characteristics are \( R_1 < 20 \Omega \) and \( C_0 < 1.5pF \).

B1, B2 version

\[ V_{DD} = 2.97 \text{ to } 3.63V, \ V_C = 0.5V_{DD}, \ V_{SS} = 0V, \ T_a = -40 \text{ to } +105^\circ C \text{ unless otherwise noted} \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC “H” level output voltage</td>
<td>( V_{\text{TOP}} )</td>
<td>measurement circuit 9, ( C_L = 15pF )</td>
<td>0.9( V_{DD} )</td>
<td>V</td>
</tr>
<tr>
<td>AC “L” level output voltage</td>
<td>( V_{\text{BASE}} )</td>
<td>measurement circuit 9, ( C_L = 15pF )</td>
<td>0.1( V_{DD} )</td>
<td>V</td>
</tr>
<tr>
<td>Duty cycle</td>
<td>Duty</td>
<td>measurement circuit 9, ( T_a = 25^\circ C, \ V_{DD} = 3.3V )</td>
<td>45</td>
<td>55</td>
</tr>
<tr>
<td>Output rise time</td>
<td>( t_r )</td>
<td>measurement circuit 9, ( C_L = 15pF, 0.1V_{DD} \rightarrow 0.9V_{DD} )</td>
<td>1.2</td>
<td>2.4</td>
</tr>
<tr>
<td>Output fall time</td>
<td>( t_f )</td>
<td>measurement circuit 9, ( C_L = 15pF, 0.9V_{DD} \rightarrow 0.1V_{DD} )</td>
<td>1.2</td>
<td>2.4</td>
</tr>
<tr>
<td>Output enable propagation delay</td>
<td>( t_{OE} )</td>
<td>measurement circuit 10, ( T_a = 25^\circ C ) INHN= “Low” \rightarrow “High” \</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Output disable propagation delay</td>
<td>( t_{OD} )</td>
<td>measurement circuit 10, ( T_a = 25^\circ C ) INHN= “High” \rightarrow “Low” \</td>
<td>200</td>
<td></td>
</tr>
</tbody>
</table>

Note: The ratings are measured by using the NPC standard crystal and jig. They may vary due to crystal characteristics, so they must be carefully evaluated. The recommended crystal element characteristics are \( R_1 < 20 \Omega \) and \( C_0 < 1.5pF \).
Timing chart

Figure 1. Output switching waveform

Figure 2. Output disable and oscillation start timing chart
FUNCTIONAL DESCRIPTION

INHN Function

Q output is stopped and becomes high impedance.

<table>
<thead>
<tr>
<th>INHN</th>
<th>Q</th>
<th>Oscillator</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH or Open</td>
<td>f_{AUT}</td>
<td>Operating</td>
</tr>
<tr>
<td>LOW</td>
<td>Hi-Z</td>
<td>Stopped</td>
</tr>
</tbody>
</table>

Power Saving Pull-up Resistor

The INHN pin pull-up resistance changes its value to $R_{PU1}$ or $R_{PU2}$ in response to the input level (HIGH or LOW).

When INHN is tied to LOW level, the pull-up resistance becomes large ($R_{PU1}$), thus reducing the current consumed by the resistance. When INHN is left open circuit or tied to HIGH level, the pull-up resistance becomes small ($R_{PU2}$), thus internal circuit of INHN becomes HIGH level.

Consequently, the IC is less susceptible to the effects of noise, helping to avoid problems such as the output stopping suddenly.

Oscillation Detection Function

The 5078 series have an oscillation detection circuit.

The oscillation detection circuit disables the output until crystal oscillation becomes stable when oscillation circuit starts up. This function avoids the abnormal oscillation in the initial power up and in a reactivation by INHN.

Boot function

It becomes easy to start oscillation by making XTN pin potential to $V_{DD}$ level when oscillation starts up. A current flows into VC pin when the voltage below a $V_{DD}$ level is being applied to VC pin. A boot function is canceled after an oscillation start.
MEASUREMENT CIRCUITS
These are measurement circuits for electrical characteristics and switching characteristics.

- Note: Bypass capacitors specified in each measurement circuit below should be connected between VDD and VSS. If the bypass capacitors are not connected, the required characteristics may not be realized.
  Circuit wiring of bypass capacitors and load capacitors should be connected as short as possible (within approximately 3mm). If the circuit wiring is long, the required characteristics may not be realized.

* The capacitor used in measurement circuits below;
  GRM188B11H103K (MURATA) 0.01μF

MEASUREMENT CIRCUIT 1
Measurement Parameter: I_{DD}, I_{STB}
MEASUREMENT CIRCUIT 2
Measurement Parameter: \( V_{OH} \), \( V_{OL} \)

\[ \begin{align*}
\text{XT input signal:} & \quad 1.5V_{p-p} \text{ sine wave} \\
\text{Signal Generator} & \quad 0.01\mu F \\
& \quad 50\Omega \\
\end{align*} \]

\[ \begin{align*}
V_{OH} & \text{ adjusted so that } \Delta V = 50 \times I_{OH} \\
V_{OL} & \text{ adjusted so that } \Delta V = 50 \times I_{OL}
\end{align*} \]

MEASUREMENT CIRCUIT 3
Measurement Parameter: \( I_Z \)

\[ \begin{align*}
\text{0.01\mu F (Ceramic Chip Capacitor)} \\
\text{0.01\mu F (Ceramic Chip Capacitor)}
\end{align*} \]
MEASUREMENT CIRCUIT 4
Measurement Parameter: \( V_{IH}, V_{IL} \)

\[
V_{IH} = V_{SS} \rightarrow V_{DD}, \text{voltage that changes enable output state}
\]
\[
V_{IL} = V_{DD} \rightarrow V_{SS}, \text{voltage that changes disable output state}
\]

MEASUREMENT CIRCUIT 5
Measurement Parameter: \( R_{PU1}, R_{PU2} \)

\[
R_{PU1} = \frac{V_{DD} - V_{INHN}}{I_{INHN}}, \quad V_{INHN} = 0V
\]
\[
R_{PU2} = \frac{V_{DD} - V_{INHN}}{I_{INHN}}, \quad V_{INHN} = 0.7V_{DD}
\]
MEASUREMENT CIRCUIT 6
Measurement Parameter: $R_{VC1}, R_{VC2}$

\[ R_{VC1} = \frac{V_{DD}}{I_{XT}} \]
\[ R_{VC2} = \frac{V_{DD}}{I_{XTN}} \]

MEASUREMENT CIRCUIT 7
Measurement Parameter: $R_{VIN}$

\[ R_{VIN} = \frac{V_{DD}}{I_{VIN}} \]
MEASUREMENT CIRCUIT 8
Measurement Parameter: $F_M$

[Diagram of Measurement Circuit 8]

MEASUREMENT CIRCUIT 9
Measurement Parameter: Duty, $t_r$, $t_f$, $V_{TOP}$, $V_{BASE}$

[Diagram of Measurement Circuit 9]
MEASUREMENT CIRCUIT 10
Measurement Parameter: $t_{OE}, t_{OD}$

- **Function Generator**: 50Ω
- **5078xx**: 0.01μF (Ceramic Chip Capacitor)
- **VDD**: 1kΩ
- **XT**: 1kΩ
- **XTN**: 1kΩ
- **INHN**: 1kΩ
- **VSS**: 1kΩ
- **VC**: $C_L = 15\text{pF}$ (Including probe capacitance)
REFERENCE DATA

The following characteristics are measured using the crystal below. Note that the characteristics will vary with the crystal used.

Crystal used for measurement

<table>
<thead>
<tr>
<th>Parameter</th>
<th>A1</th>
<th>B1</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{osc}}$(MHz)</td>
<td>77.76</td>
<td>155.52</td>
</tr>
<tr>
<td>$C_0$(pF)</td>
<td>2.4</td>
<td>1.5</td>
</tr>
<tr>
<td>$\gamma$($=C_0/C_1)$</td>
<td>290</td>
<td>330</td>
</tr>
<tr>
<td>$R_1$(Ω)</td>
<td>7.0</td>
<td>9.3</td>
</tr>
</tbody>
</table>

Pulling Range

[Measurement conditions] $V_{\text{DD}}$=3.3V, $V_{\text{SS}}$=0V, $T_a$=25°C

[5078Ax] $f_{\text{osc}}$=77.76MHz

[5078Bx] $f_{\text{osc}}$=155.52MHz

[Measurement circuit diagram]
Phase Noise

[Measurement conditions] \( V_{DD}=3.3V, V_{SS}=0V, T_a=25^\circ C \)

\[
\begin{align*}
\text{[5078A1]} & \ f_{OSC}=77.76MHz, f_{OUT}=77.76MHz \\
\text{[5078A2]} & \ f_{OSC}=77.76MHz, f_{OUT}=38.88MHz
\end{align*}
\]

\[
\begin{align*}
\text{[5078B1]} & \ f_{OSC}=155.52MHz, f_{OUT}=155.52MHz \\
\text{[5078B2]} & \ f_{OSC}=155.52MHz, f_{OUT}=77.76MHz
\end{align*}
\]

Rms jitter (12kHz~20MHz)
- VC=0V : 100fs
- VC=1.65V : 77fs
- VC=3.3V : 71fs

\[
\begin{align*}
\text{[5078B1]} & \ f_{OSC}=155.52MHz, f_{OUT}=155.52MHz \\
\text{[5078B2]} & \ f_{OSC}=155.52MHz, f_{OUT}=77.76MHz
\end{align*}
\]

Rms jitter (12kHz~20MHz)
- VC=0V : 181fs
- VC=1.65V : 140fs
- VC=3.3V : 130fs

\[
\begin{align*}
\text{[5078B1]} & \ f_{OSC}=155.52MHz, f_{OUT}=155.52MHz \\
\text{[5078B2]} & \ f_{OSC}=155.52MHz, f_{OUT}=77.76MHz
\end{align*}
\]

Rms jitter (12kHz~20MHz)
- VC=0V : 72fs
- VC=1.65V : 51fs
- VC=3.3V : 46fs

\[
\begin{align*}
\text{[5078B1]} & \ f_{OSC}=155.52MHz, f_{OUT}=155.52MHz \\
\text{[5078B2]} & \ f_{OSC}=155.52MHz, f_{OUT}=77.76MHz
\end{align*}
\]

Rms jitter (12kHz~20MHz)
- VC=0V : 140fs
- VC=1.65V : 106fs
- VC=3.3V : 97fs

[Measurement circuit diagram]
Modulation Bandwidth

[Measurement conditions] \(V_{DD}=3.3V\), \(V_{SS}=0V\), \(T_a=25^\circ C\)

\[5078A1\] \(f_{OSC}=77.76MHz\), \(f_{OUT}=77.76MHz\)

\[5078A2\] \(f_{OSC}=77.76MHz\), \(f_{OUT}=38.88MHz\)

\[5078B1\] \(f_{OSC}=155.52MHz\), \(f_{OUT}=155.52MHz\)

\[5078B2\] \(f_{OSC}=155.52MHz\), \(f_{OUT}=77.76MHz\)

[Measurement circuit diagram] Measurement circuit 8
**Negative Resistance**

[Measurement conditions] \( V_{DD}=3.3\,\text{V}, \, V_{SS}=0\,\text{V}, \, T_a=25\,\text{°C}, \, C_0=0\,\text{pF} \)

At the time of oscillation start, negative resistance becomes deep by boot function. The boot function is released when the oscillation is steady, and oscillation starts.

[Measurement circuit diagram]

![Circuit Diagram](image)

Measurement results using 4396B Agilent analyzer on NPC test jig. Measurements will vary with test jig and measurement environment.
**Drive Level**

[Measurement conditions] \( V_{DD} = 3.3 \text{V}, V_{SS} = 0 \text{V}, T_a = 25^\circ\text{C} \)

\[ 5078\text{Ax} \] \( f_{OSC} = 77.76 \text{MHz} \)

\[ 5078\text{Bx} \] \( f_{OSC} = 155.52 \text{MHz} \)

[Measurement circuit diagram]

\[ DL = (I_{Xtal})^2 \times \text{Re} \]

\( \text{IXtal: Current through Crystal (RMS)} \)

\( \text{Re: Crystal’s effective resistance} \)

\( C_L = 15 \text{pF} \)
Oscillator CL Characteristics

[Measurement conditions] \( V_{DD} = 3.3V, V_{SS} = 0V, T_a = 25^\circ C \)

**[5078Ax]** \( f_{OSC} = 77.76MHz \)

**[5078Bx]** \( f_{OSC} = 155.52MHz \)

[Measurement circuit diagram]

\[
C_{LOSC} = \frac{C1}{\left( \frac{f_{OSC}}{f_s} \right)^2} - C0
\]

- **C1**: Crystal element equivalent series capacitance
- **C0**: Crystal element equivalent parallel capacitance
- **f_s**: Crystal element series resonance frequency

\( C_{LOSC} \): Oscillator circuit equivalent capacitance determined by oscillator frequency

0.01\( \mu \)F (Ceramic Chip Capacitor)
VC Terminal Input Impedance

[Measurement conditions] $T_a=25^\circ C$, $V_C=0V$

[5078Ax]

[5078Bx]

[Measurement circuit diagram]
Current Consumption

[Measurement conditions] \( V_{DD} = 3.3V, V_{SS} = 0V, T_a = 25^\circ C \)

5078 series

[Measurement circuit diagram] Measurement circuit 1
Output Waveform

[Measurement conditions] \( V_{DD} = 3.3 \text{V} \), \( V_{SS} = 0 \text{V} \), \( V_C = 1.65 \text{V} \), \( T_a = 25 \text{°C} \)

\[5078A1\] \( f_{OSC} = 77.76 \text{MHz} \), \( f_{OUT} = 77.76 \text{MHz} \)

\[5078A2\] \( f_{OSC} = 77.76 \text{MHz} \), \( f_{OUT} = 38.88 \text{MHz} \)

\[5078B1\] \( f_{OSC} = 155.52 \text{MHz} \), \( f_{OUT} = 155.52 \text{MHz} \)

\[5078B2\] \( f_{OSC} = 155.52 \text{MHz} \), \( f_{OUT} = 77.76 \text{MHz} \)

[Measurement circuit diagram] Measurement circuit 9

Measurement equipment: Oscilloscope DSO80604B (Agilent), Differential probe 1134A (Probe head E2678A)
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SEIKO NPC CORPORATION
1-9-9, Hatchobori, Chuo-ku,
Tokyo 104-0032, Japan
Telephone: +81-3-5541-6501
Facsimile: +81-3-5541-6510
http://www.npc.co.jp/
Email:sales@npc.co.jp