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Editing 8-channel DSD Signals Using NPC SM5951A as Example

(Part.2)

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In the previous issue, we discussed the general topics of editing of the DSD signal. In this issue, the specific functions and characteristics of the SM5951AF are given.

Features and functions of SM5951AF

Figure 9 shows the block diagram of SM5951AF. Based on this figure, the features and functions of the SM5951AF are explained as follows.

(1) Multi-channel support

SM5951AF incorporates eight channels of editing units to support a multiple-input mixing, and each unit can edit four channels of input DSD signals. This IC alone can edit 32 channels of input DSD signals and eight channels of output DSD signals.

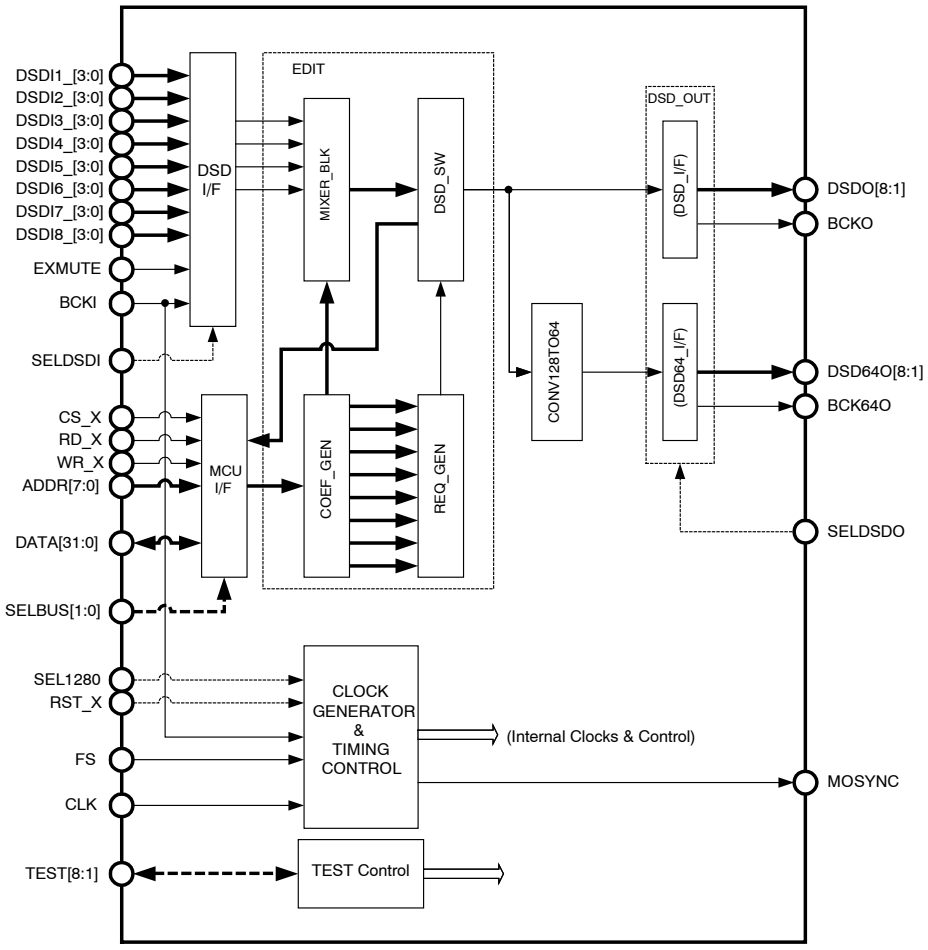
In the block diagram in Figure 9, pins DSDI1_[3:0] to DSDI8_[3:0] at the upper left part input 32 channels of DSD signals. These signals are edited by the editing block of eight channels at the center (enclosed by the dotted line and indicated as EDIT), and the edited signals are output to pins DSDO[8:1] via DSD_I/F block.

(2) Supporting both $128f_S/64f_S$

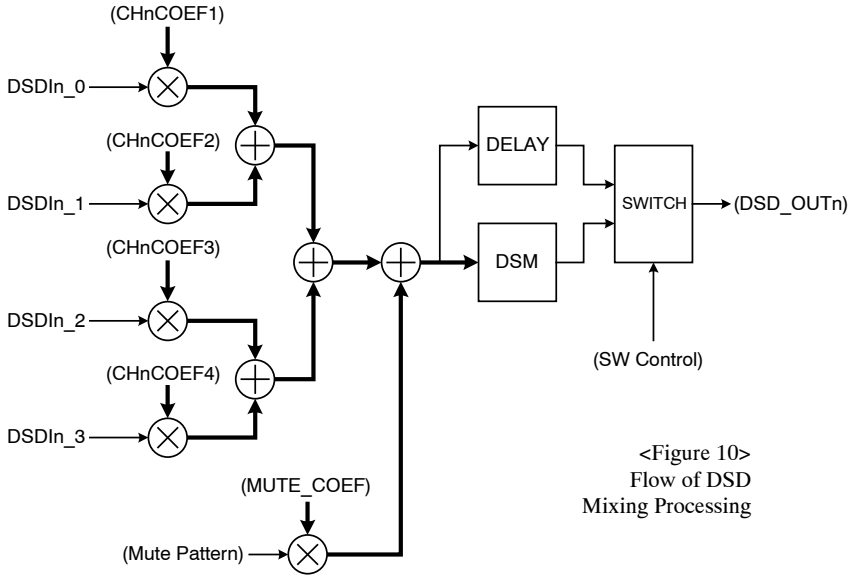
The sample rate of the DSD signal supports not only $64f_S$ of the ordinary SA-CD but also double sampling rate of SA-CD ($128f_S$), offering the possibility for high-accuracy recording and mastering. By using the $128f_S$ mode, the rising frequency of the shaping curve of the quantization noise of ΔΣ conversion can be shifted to 40kHz from about 20kHz in the $64f_S$ mode. As a result, a ΔΣ converter can be realized with a signal band in which a dynamic range (DR) of 120dB or more can be secured is about 40kHz.

By using this expanded signal band, penetration of noise into the signal band can be minimized during signal processing, such as filtering and ΔΣ conversion that are essential for DSD editing.

In the $128f_S$ mode, signals can also be output at a downsampled $64f_S$ rate, as well as $128f_S$ output. In addition, the contents recorded or mastered in $128f_S$ DSD can also be converted for SA-CD.



<Figure 9> Block Diagram of 8-ch DSD Editing IC SM5951A of NPC



<Figure 10>
Flow of DSD
Mixing Processing

In Figure 9, block CONV 128 TO 64 shown at the center right part is the conversion unit, and $64f_S$ data can also be output to the DSD 64 O[8:1] pins at the same time.

(3) Auto-bypass function minimizing sound quality degradation

Figure 10 shows the flow of mixing processing of four signals of one channel by the editing block. The input four DSD signals are multiplied by a coefficient set corresponding to each signal and determined by each DSD sample rate, and then summed up (mixed). The DSM block in the subsequent stage performs 5th order ΔΣ modulation (noise shaping) on the mixed signal to convert it into a DSD signal again.

Simultaneously, input signal before modulation is appended the same delay as the ΔΣ modulator and is transferred to the SWITCH block in the succeeding stage.

For editing processing a function to select and output one of the four signals is necessary. To do this, it is ideal to mute the other three signals gradually and to output only one DSD signal as it has been input.

SM5951AF can make an ideal signal switching like this. The DELAY block and SWITCH block of this IC are to select a delayed DSD signal automatically.

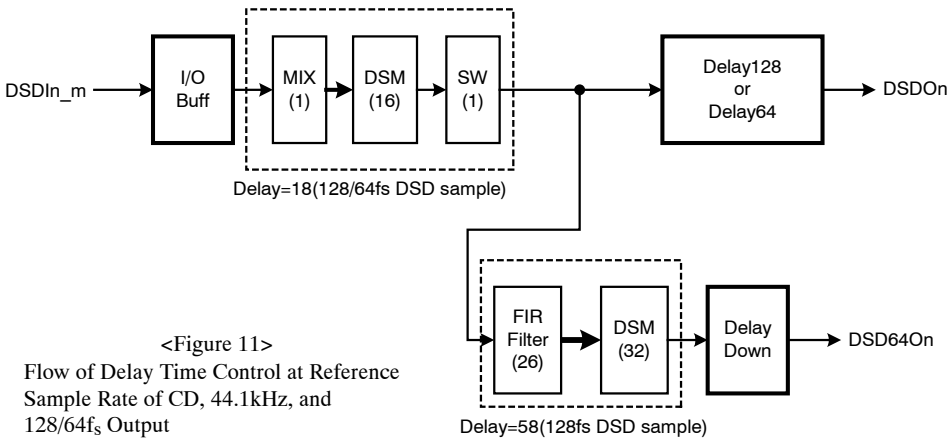
In doing so, energy accumulated in the integrator of ΔΣ modulator is gradually release for audible noise cancellation. In the end, the selected signal is verified against a DSD pattern in a specific period, so that it is switched without any audible noise. This is "auto bypassing to the original signal" that minimizes the degradation of the sound quality and is the biggest feature of the SM5951AF.

The mute signal of DSD that alternating 1 and 0 is treated by means of auto-bypass processing in the same manner as the DSD signals of the other channels. The mute status is automatically recognized from the value of each coefficient, and the original signal is automatically converted into an internal DSD mute signal of 96h (1001-0110) in HEX code of the ΔΣ modulator without idling noise, or into a DSD mute signal with a duty of 50% that is input from an external source, with very little noise generated.

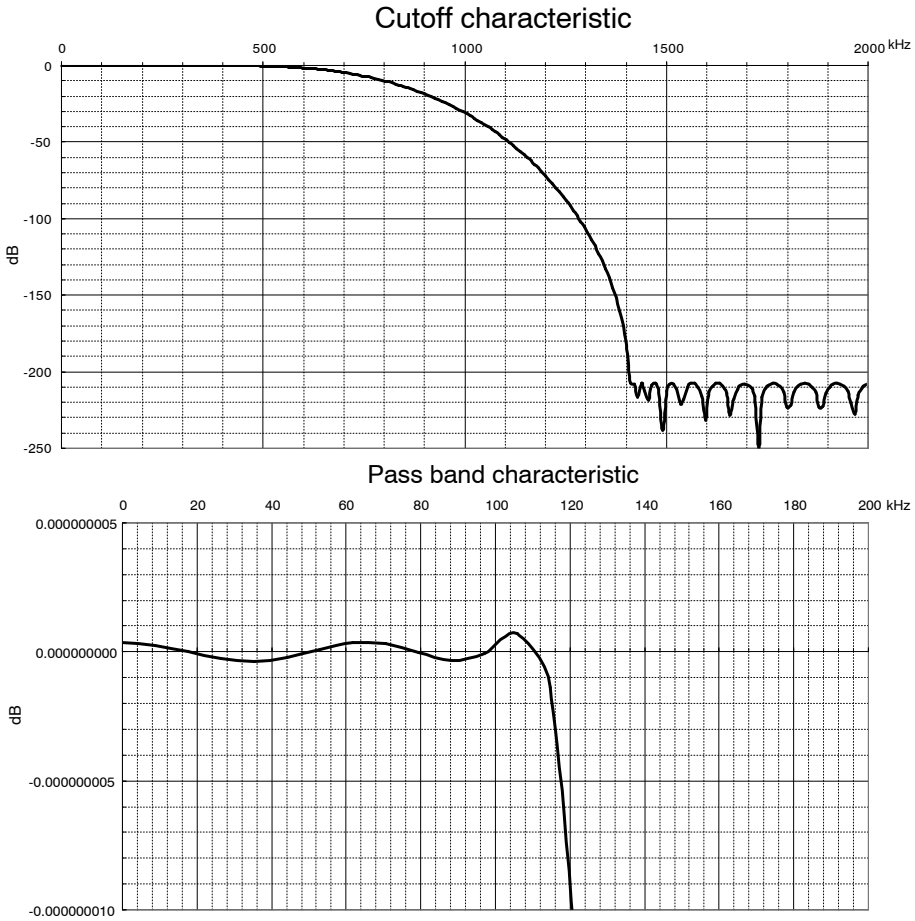
(4) Internal delay adjustment function that can clearly define editing timing

For professional audio application, it is very important to manage the delays of a signal at 44.1 kHz, the reference sample rate unit same as that of a CD. When signal processing or ΔΣ modulation processing is performed when a DSD signal is edited, interim delay is generated. As it is, the delay relation of the signal is disturbed, causing degradation of the signal such as a phase shift.

To prevent this, the delay of the output signals of all the eight channels can be adjusted in units of the reference sample rate. Figure 11 shows the flow of the delay control block and of outputting both the $128f_S$ and $64f_S$



<Figure 11>
Flow of Delay Time Control at Reference Sample Rate of CD, 44.1kHz, and $128/64f_S$ Output



<Figure 12> Characteristics of FIR Filter for $128f_S$-to-$64f_S$ Conversion

(5) 64fs output retaining wide signal band as is

When the sample rate is converted from $128f_S$ to $64f_S$, a FIR filter prevent the aliasing noise resulting from downsampling. Figure 12 shows the calculated characteristics of this FIR filter. As the cutoff characteristics, stop band is attenuated by -200dB to half of $64f_S$, 1.4112MHz, demonstrating that influence of aliasing is negligible. Even in the pass band, the ripple characteristic is within ±0.000000001dB over 100kHz band and any attenuation to the signal component is not detected.

Test and evaluation results of SM5951AF

The results of testing and evaluating the SM5951AF are shown next.

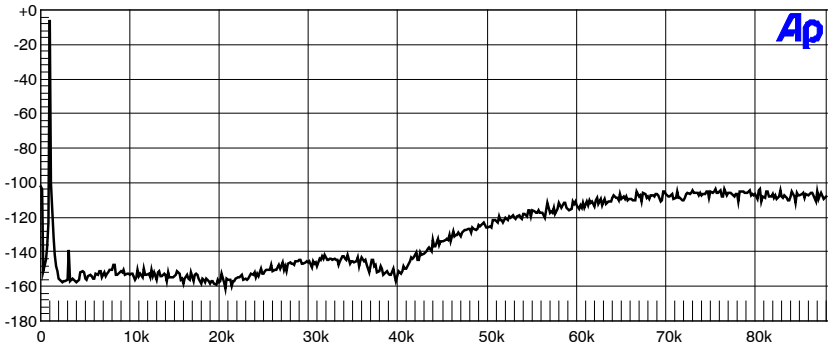
(1) Output characteristic

Figures 13 and 14 show the output characteristics actually measured in the $128f_S$ mode and $64f_S$ mode, respectively. The input signals are supplied from an audio analyzer of Audio Precision. A sine wave of 1kHz, 0dB is generated, on which PCM-DSD modulation is performed at a modulation rate of 50% by FPGA. The resultant signal is input to the SM5951AF.

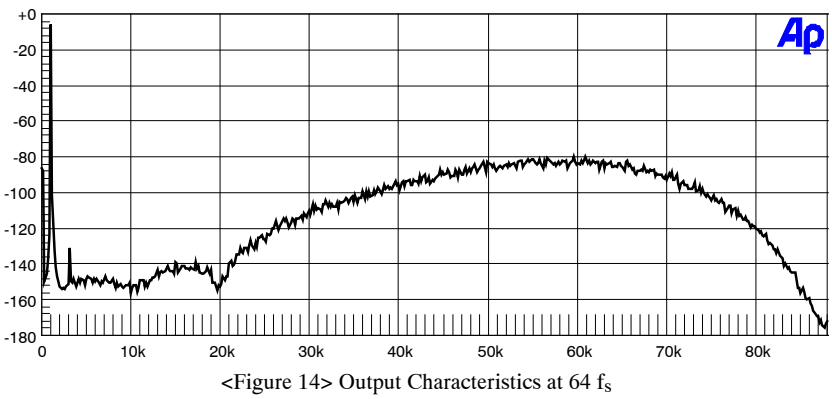
The DSD output of the SM5951AF cannot be input to the audio analyzer as is. Therefore, it is converted into a PCM signal of $4f_S$ by using the NPC's DSD-PCM converter SM5819AF, and FFT is performed on the converted signal by using the audio analyzer again. Although the SM5819AF does not support $128f_S$, measurement was performed by operating the converter in $2f_S$ mode at $1024f_S$, two times the original oscillation, knowing that such a operation clock is out of the specification range.

Figure 13 shows shaping curve characteristic demonstrating -140 dB or less in a band up to 40kHz.

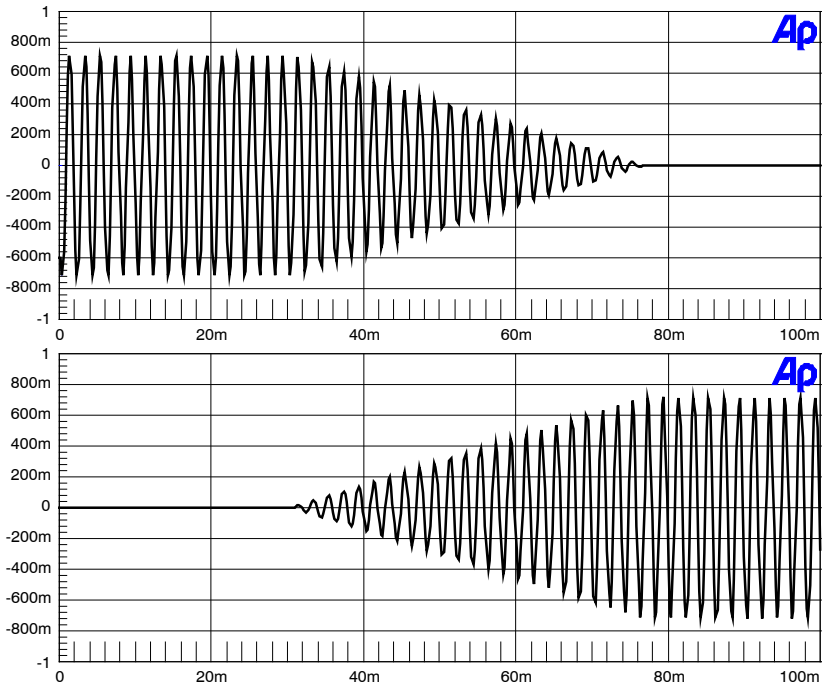
In Figure 14, the $4f_S$ mode of the SM5819AF is used as is, and the shaping curve characteristic of $64f_S$ is shown as is without influence of aliasing noise.



<Figure 13> Output Characteristics at 128 f_S



<Figure 14> Output Characteristics at 64 f_S

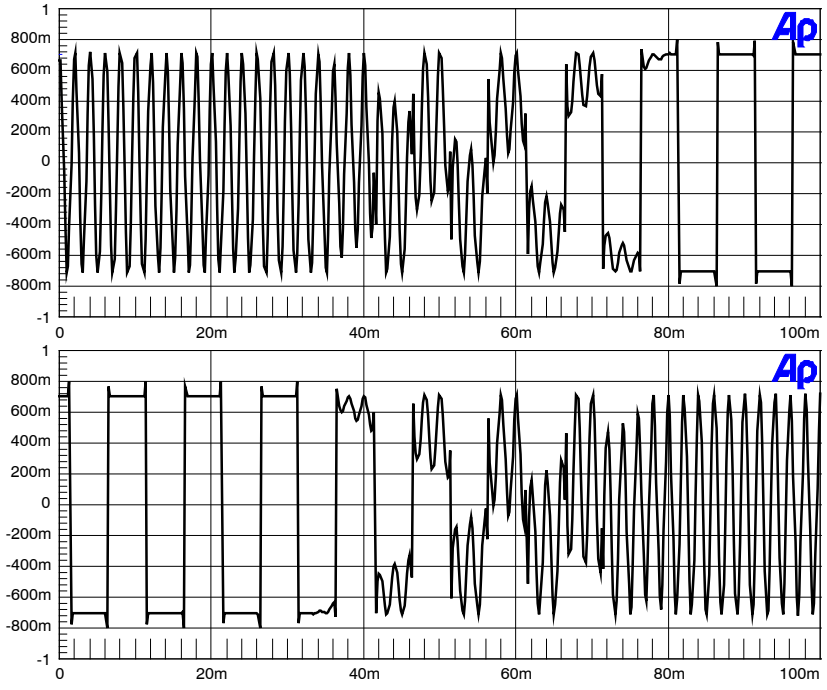


<Figure 15> Cross-fade of 500Hz Sine Wave vs. 96h-Mute (1)

(2) Cross-fade waveform

Next, two types of waveforms of cross-fade operation that gradually switches two input signals are shown. This is done with the same connection condition as above, and the $4f_S$ output of the SM5891AF is monitored in the $64f_S$ mode of DSD rate. Both Figures 15 and 16 show the result of monitoring the edited output of two channels with two input channels, and the input signals are exchanged at the top and bottom of the figure for cross-fading.

In Figure 15, a sine wave of 500Hz, 0dB is cross-faded to a 96h-DSD mute pattern with the channel shown at the top of the figure. This is reversed with the channel at the bottom. In Figure 16, a sine wave of 500Hz, 0dB is cross-faded to a rectangular wave of 100Hz, which is reversed with the channel at the bottom.



<Figure 16> Cross-fade of 500Hz Sine Wave vs. 100Hz Rectangular Wave (2)

(3) Auto-bypass operation

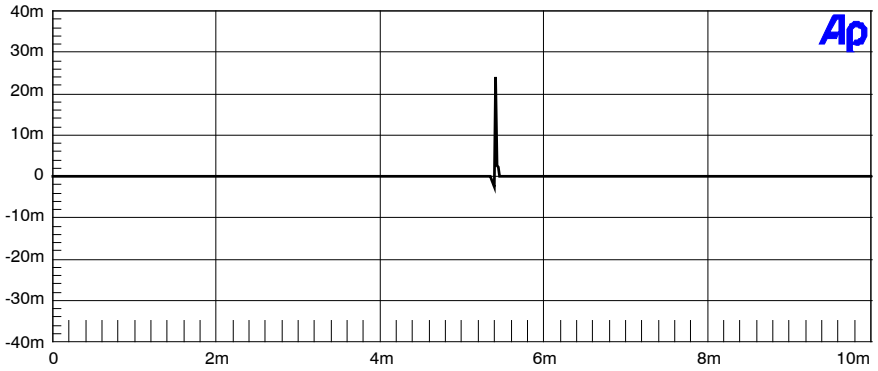
The biggest feature of the SM5951AF is the effect of its auto-bypass function. This is switching between DSD mute patterns that should be inaudible if switching goes well.

Because a DSD signal has only two values as levels, ±1, the weight of the 1 bit has a serious influence. Especially, a DSD mute pattern like 96h generates unacceptable pulse noise even if it is occasionally shifted 1 bit, at the very instant the pattern is changed. Figure 17 shows the noise that is generated when a DSD mute pattern of 96h is forced to change to a 1-bit shifted pattern in the stream.

Whereas the amplitude of the sine wave of DSD 0dB (modulated 50%) in Figure 16 is about 700m (note: unit expression of signal level ratio with respect to the full scale of the audio analyzer, and m indicates milli and μ indicates micro) (Figure 16), the noise level in Figure 17 reaches 24m. If this is converted into decibels, noise of as high as -30dB (20log(24/700) = -29.2dB) is generated even momentarily.

Figure 18 shows the result of switching the signal via the SM591AF. The scale is the same as in Figure 17 but the bottom of Figure 18 shows the expanded view because the waveform is barely visible. The internal operation at this time is this: no AC noise is generated from time 0 ms to 28ms at which the signal is switched, and the DSD mute pattern of 96h appears as is.

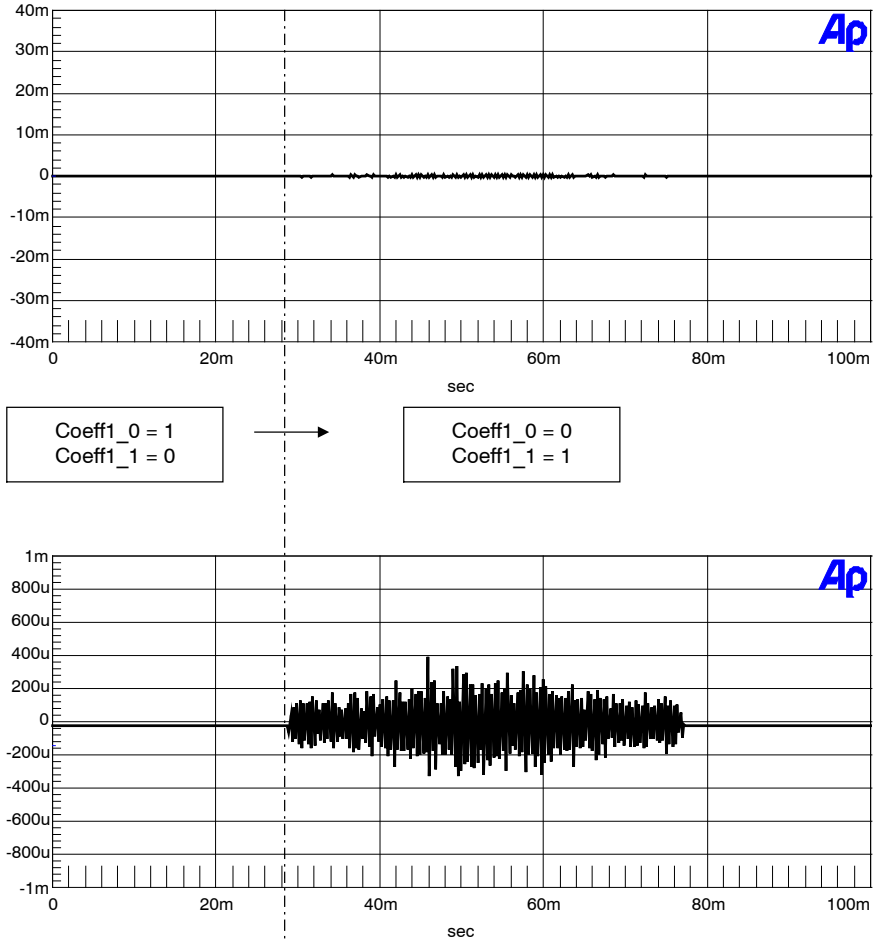
At time 28ms when the pattern is switched to a signal shifted 1 bit, the internal ΔΣ modulator starts a noise shaping operation, and noise dependent upon the shaping curve is generated. Afterward, the noise energy accumulated in the ΔΣ modulator gradually decreases, pattern matching is confirmed, and the signal is changed to 96h DSD mute pattern shifted 1 bit itself at time around 76ms.



<Figure 17> Noise when Signal is forced to switch without any processing

At this point, idling noise of the ΔΣ modulator is perfectly eliminated. Although noise is generated at time of 28ms, the instance the signal has been changed, to 76ms, this amplitude level is around 200μ, indicating that the noise has decreased to about 1/100. This waveform shows the effect of the auto-bypass function best.

By using this SM5951AF, a high-accuracy DSD mixing system of multiple channels can be configured with relative ease. NPC believes that it helps increase high-quality music source of multi-channel SA-CD.



<Figure 18> Mute Noise when Signal is switched through SM5951AF

In the 116th AES Convention held in Berlin, Euphonix exhibited 128 f_S DSD supporting the "System 5" digital mixing console that is equipped with Sony Oxford's signal processing board, "Mix Engine." This indicates that movements to support 128f_S DSD have already started in the production equipment industry.

Philips Electronics exhibited "SA-CD Creator Pack" including DSD master creating plug-in software for Digital Audio Workstation "ProTools" which is widely used in music production, eliciting much attention from its users. As a result, the future sales of SA-CD titles may be spurred.

From these facts at recent AES Convention, it is expected that a multi-track recorder using SM5951AF and supporting 128f_S DSD will be developed in the near future.

Finally, we would like to express our gratitude to those who at the SACD Business Center of Sony Corporation who extended technological cooperation to us in developing this LSI.

(Nippon Precision Circuits, Inc.)